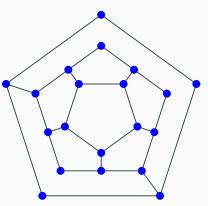
Pre-lecture brain teaser

Does this graph have a Hamiltonian cycle?



a Yes.

b No.

Answer: B. The outer cycle has two entrances/exits that aren't next to each other always leaving out one or two vertices.

ECE-374-B: Lecture 21 - Lots of NP-Complete reductions

Instructor: Abhishek Kumar Umrawal

November 9, 2022

University of Illinois at Urbana-Champaign

Today

NP-Completeness of the following two problems.

- Hamiltonian cycle
- 3-coloring

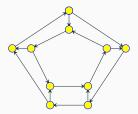
Important: Understanding the problems and that they are hard.

Proofs and reductions will be sketchy and mainly to give a flavor.

Reduction from 3SAT to Hamiltonian Cycle

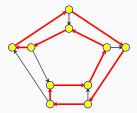
Input Given a directed graph G = (V, E) with *n* vertices. Goal Does *G* have a Hamiltonian cycle?

• A Hamiltonian cycle is a cycle in the graph that visits every vertex in *G* exactly once.

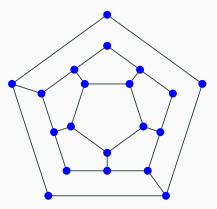


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Is the following graph Hamiltonianan?



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Directed Hamiltonian Cycle is NP-Complete

- Directed Hamiltonian Cycle is in NP: exercise.
- Hardness: We will show the following.

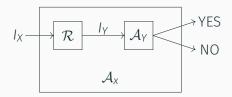
3-SAT \leq_P Directed Hamiltonian Cycle

Directed Hamiltonian Cycle is NP-Complete

- Directed Hamiltonian Cycle is in NP: exercise.
- Hardness: We will show the following.

3-SAT \leq_P Directed Hamiltonian Cycle

We have the following reduction diagram.



Reduction

Given 3-SAT formula φ create a graph G_{φ} such that the following hold.

- + G_{φ} has a Hamiltonian cycle if and only if φ is satisfiable.
- G_{φ} should be constructible from φ by a polynomial time algorithm \mathcal{A} .

Notation: φ has *n* variables x_1, x_2, \ldots, x_n and *m* clauses C_1, C_2, \ldots, C_m .

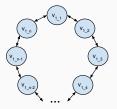
Reduction: First Ideas

- Viewing SAT: Assign values to *n* variables, and each clauses has 3 ways in which it can be satisfied.
- Construct graph with 2ⁿ Hamiltonian cycles, where each cycle corresponds to some boolean assignment.
- Then add more graph structure to encode constraints on assignments imposed by the clauses.

$$f(x_1) = 1 \tag{1}$$

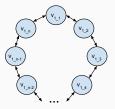
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We create a cyclic graph that always has a Hamiltonian cycle.



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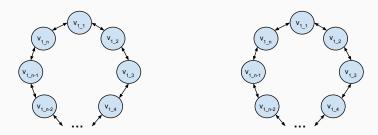
We create a cyclic graph that always has a Hamiltonian cycle.



But how do we encode the variable?

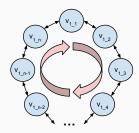
$$f(x_1) = 1$$

Maybe we can encode the variable x_1 in terms of the cycle direction.

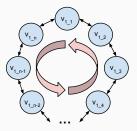


$$f(x_1) = 1$$

Maybe we can encode the variable x_1 in terms of the cycle direction.



If $x_1 = 1$



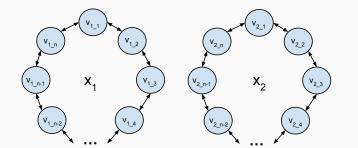
If $x_1 = 0$

$$f(x_1, x_2) = 1$$
 (2)

Maybe two circles? Now we need to connect them so that we have a single Hamiltonian cycle.

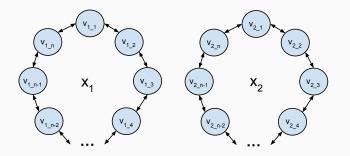
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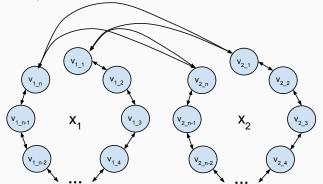
$$f(x_1, x_2) = 1$$
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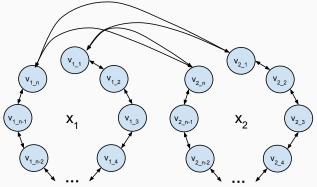
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How do we encode multiple variables?

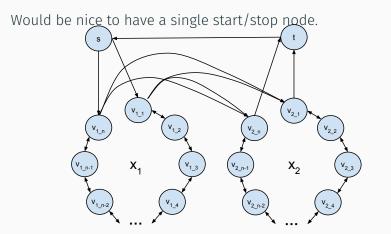
$$f(x_1, x_2) = 1$$
 (4)

Would be nice to have a single start/stop node.



How do we encode multiple variables?

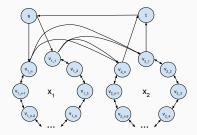
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How do we encode multiple variables?

$$f(x_1, x_2) = 1$$
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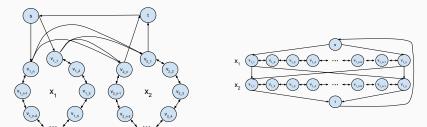
Getting a bit messy. Let's reorganize as follows.



How do we encode multiple variables?

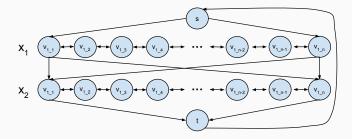
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Getting a bit messy. Let's reorganize as follows.



$$f(x_1, x_2) = 1$$
 (6)

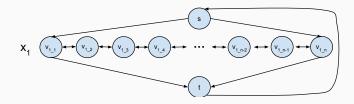
This is how we encode variable assignments in a variable loop!



How do we handle clauses?

$$f(x_1) = x_1 \tag{7}$$

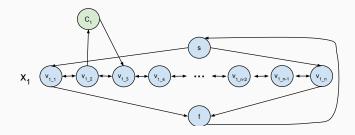
Lets go back to our one variable graph.



How do we handle clauses?

$$f(x_1) = x_1 \tag{8}$$

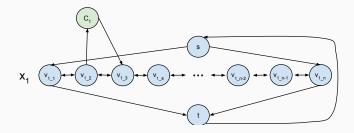
Add node for clause.



How do we handle clauses?

$$f(x_1, x_2) = (x_1 \vee \overline{x_2}) \tag{9}$$

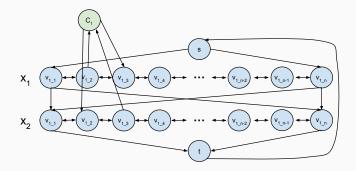
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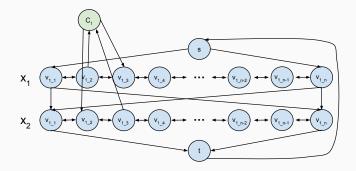
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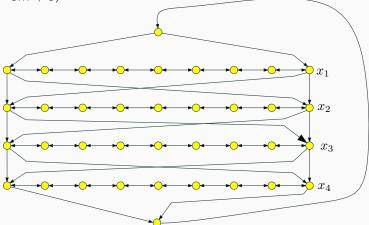
$$f(x_1, x_2) = (x_1 \lor \overline{x_2}) \land (\overline{x_1} \lor x_2)$$
(10)

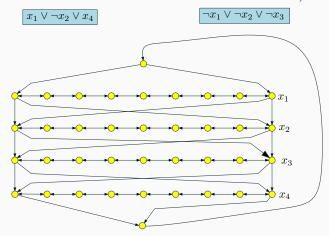
What if the expression has multiple clauses:

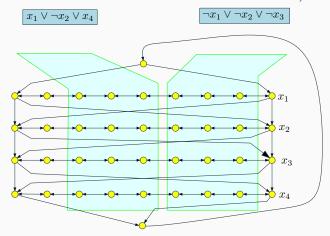


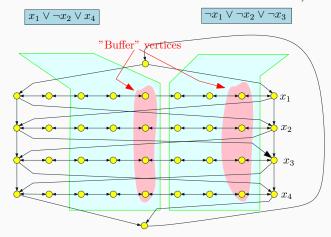
The Reduction: Review I

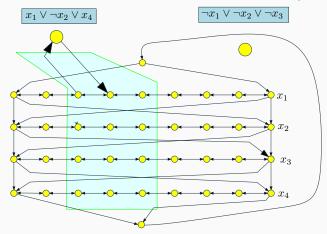
- Traverse path *i* from left to right iff x_i is set to true
- Each path has 3(m + 1) nodes where m is number of clauses in φ; nodes numbered from left to right (1 to 3m + 3)





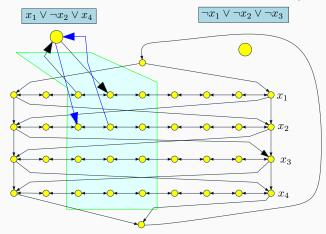






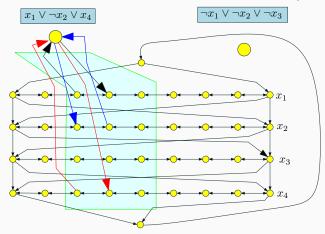
The Reduction algorithm: Review II

Add vertex c_j for clause C_j . c_j has edge from vertex 3j and to vertex 3j + 1 on path *i* if x_i appears in clause C_j , and has edge from vertex 3j + 1 and to vertex 3j if $\neg x_i$ appears in C_j .



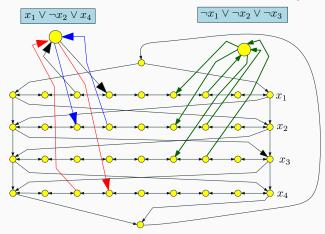
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Theorem

 φ has a satisfying assignment iff ${\rm G}_{\varphi}$ has a Hamiltonian cycle.

Based on proving the following two lemmas.

Lemma If φ has a satisfying assignment then G_{φ} has a Hamilton cycle.

Lemma

If G_{φ} has a Hamilton cycle then φ has a satisfying assignment.

Lemma

If φ has a satisfying assignment then ${\sf G}_{\varphi}$ has a Hamilton cycle.

Proof.

- ⇒ Let *a* be the satisfying assignment for φ . Define Hamiltonian cycle as follows.
 - If $a(x_i) = 1$ then traverse path *i* from left to right.
 - If $a(x_i) = 0$ then traverse path *i* from right to left.
 - For each clause, path of at least one variable is in the "right" direction to splice in the node corresponding to clause.

Suppose Π is a Hamiltonian cycle in G_{φ} .

Definition

We say Π is *canonical* if for each clause vertex c_j the edge of Π entering c_j and edge of Π leaving c_j are from the same path corresponding to some variable x_i . Otherwise Π is *non-canonical* or emphcheating.

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Lemma Every Hamilton cycle in G_{φ} is canonical.

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Every Hamilton cycle in G_{φ} is canonical.

- If Π enters c_j (vertex for clause C_j) from vertex 3j on path i then it must leave the clause vertex on edge to 3j + 1 on the same path i.
 - If not, then only unvisited neighbor of 3j + 1 on path *i* is 3j + 2.
 - Thus, we don't have two unvisited neighbors (one to enter from, and the other to leave) to have a Hamiltonian Cycle.
- Similarly, if Π enters c_j from vertex 3j + 1 on path *i* then it must leave the clause vertex c_j on edge to 3j on path *i*.

Lemma

Any canonical Hamilton cycle in G_{φ} corresponds to a satisfying truth assignment to φ .

Consider a canonical Hamilton cycle Π .

- For every clause vertex c_j , vertices visited immediately before and after c_j are connected by an edge on same path corresponding to some variable x_j .
- We can remove c_j from cycle, and get Hamiltonian cycle in $G c_j$.
- Hamiltonian cycle from Π in $G \{c_1, \ldots c_m\}$ traverses each path in only one direction, which determines truth assignment.
- Easy to verify that this truth assignment satisfies φ .

Hamiltonian cycle in undirected graph

Problem

Input Given undirected graph G = (V, E).

Goal Does G have a Hamiltonian cycle? That is, is there a cycle that visits every vertex exactly one (except start and end vertex)?

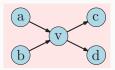
Theorem *Hamiltonian cycle* problem for undirected graphs is NP-Complete.

Proof.

- The problem is in **NP**; proof left as exercise.
- Hardness proved by reducing Directed Hamiltonian Cycle to this problem.

Reduction

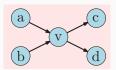
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Reduction

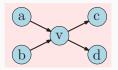
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• Replace each vertex v by 3 vertices: v_{in} , v, and v_{out} .



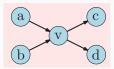
Reduction

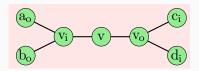
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- A directed edge (a, b) is replaced by edge (a_{out}, b_{in}) .



Reduction

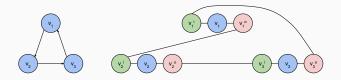
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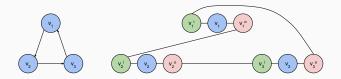
Reduction Sketch Example

Graph with cycle:

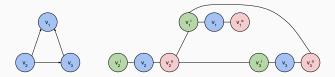


Reduction Sketch Example

Graph with cycle:



Graph without cycle:



Reduction: Wrapup

- The reduction is polynomial time: exercise.
- The reduction is correct: exercise.

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Easy to modify the reduction from **3-SAT** to **Halitonian Cycle** or do a reduction from **Halitonian Cycle**.

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Implies that Longest Simple Path in a graph is NP-Complete.

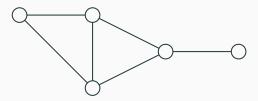
NP-Completeness of Graph Coloring

Problem: Graph Coloring

Instance: G = (V, E): Undirected graph, integer k. **Question:** Can the vertices of the graph be colored using k colors so that vertices connected by an edge do not get the same color?

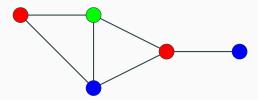
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Observation: If *G* is colored with *k* colors then each color class (nodes of same color) form an independent set in *G*. Thus, *G* can be partitioned into *k* independent sets iff *G* is *k*-colorable.

Graph 2-Coloring can be decided in polynomial time.

G is 2-colorable iff *G* is bipartite! There is a linear time algorithm to check if *G* is bipartite using breadth first search.

Problems related to graph coloring

Register Allocation

Assign variables to (at most) *k* registers such that variables needed at the same time are not assigned to the same register.

Interference Graph

Vertices are variables, and there is an edge between two vertices, if the two variables are "live" at the same time.

Observations

- [Chaitin] Register allocation problem is equivalent to coloring the interference graph with *k* colors.
- Moreover, 3-COLOR $\leq_P k$ Register Allocation, for any $k \geq 3$.

Given *n* classes and their meeting times, are *k* rooms sufficient?

Reduce to Graph *k*-Coloring problem.

Create graph G

- a node v_i for each class *i*.
- an edge between v_i and v_j if classes *i* and *j* conflict.

Exercise: G is k-colorable iff k rooms are sufficient.

Cellular telephone systems that use Frequency Division Multiple Access (FDMA) (example: GSM in Europe and Asia and AT&T in USA).

- Breakup a frequency range [a, b] into disjoint *bands* of frequencies $[a_0, b_0], [a_1, b_1], \ldots, [a_k, b_k]$.
- Each cell phone tower (simplifying) gets one band.
- Constraint: nearby towers cannot be assigned same band, otherwise signals will interference.

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- Each cell phone tower (simplifying) gets one band.
- Constraint: nearby towers cannot be assigned same band, otherwise signals will interference.

Problem: given *k* bands and some region with *n* towers, is there a way to assign the bands to avoid interference?

Can reduce to *k*-coloring by creating interference/conflict graph on towers.

Showing hardness of 3 COLORING

3-Coloring is NP-Complete

- 3-Coloring is in NP.
 - Non-deterministically guess a 3-coloring for each node
 - Check if for each edge (*u*, *v*), the color of *u* is different from that of *v*.
- Hardness: We will show 3-SAT \leq_P 3-Coloring.

Start with **3SAT** formula (i.e., 3CNF formula) φ with *n* variables x_1, \ldots, x_n and *m* clauses C_1, \ldots, C_m . Create graph G_{φ} such that G_{φ} is 3-colorable iff φ is satisfiable.

- need to establish truth assignment for x_1, \ldots, x_n via colors for some nodes in G_{φ} .
- create triangle with node True, False, Base.
- for each variable x_i two nodes v_i and \overline{v}_i connected in a triangle with common Base.
- If graph is 3-colored, either v_i or $\bar{v_i}$ gets the same color as True. Interpret this as a truth assignment to v_i .
- Need to add constraints to ensure clauses are satisfied (next phase).

We want to create a gadget that:

- Is 3 colorable if at least one of the literals is true.
- Not 3-colorable if none of the literals are true.

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Let's start off with the simplest SAT we can think of:

$$f(x_1, x_2) = (x_1 \lor x_2)$$
(11)

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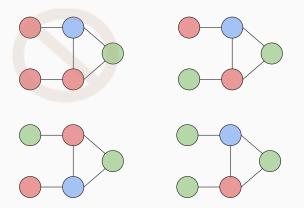
Assume green=true and red=false,

- Is 3 colorable if at least one of the literals is true
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Let's try some stuff:

- Is 3 colorable if at least one of the literals is true
- Not 3-colorable if none of the literals are true

Seems to work:



- Is 3 colorable if at least one of the literals is true.
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- Is 3 colorable if at least one of the literals is true.
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How do we do the same thing for 3 variables?

$$f(x_1, x_2, x_3) = (x_1 \lor x_2 \lor x_3)$$
(12)

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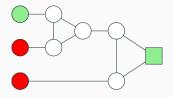
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3 color this gadget II

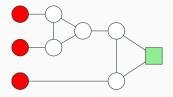
You are given three colors: red, green and blue. Can the following graph be three colored in a valid way (assuming that some of the nodes are already colored as indicated).



a Yes.

b No.

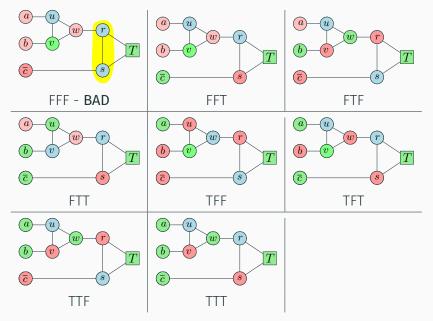
You are given three colors: red, green and blue. Can the following graph be three colored in a valid way (assuming that some of the nodes are already colored as indicated).



a Yes.

b No.

3-coloring of the clause gadget

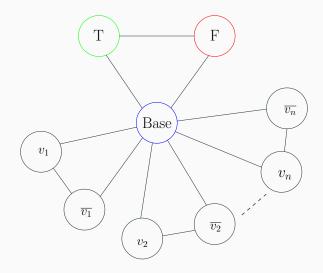


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Next we need a gadget that assigns literals. Our previously constructed gadget assumes the following.

- All literals are either red or green.
- Need to limit graph so only x_1 or $\overline{x_1}$ is green. Other must be red.

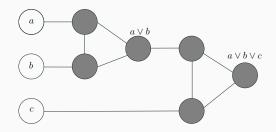
Reduction Idea II - Literal Assignment II



For each clause $C_j = (a \lor b \lor c)$, create a small gadget. graph

- Gadget graph connects to nodes corresponding to *a*, *b*, *c*.
- Needs to implement OR.

OR-gadget-graph:

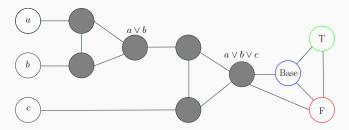


Property: If *a*, *b*, *c* are colored False in a 3-coloring then output node of OR-gadget has to be colored False.

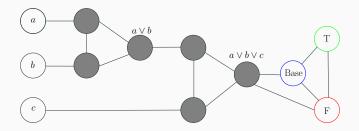
Property: If one of a, b, c is colored True then OR-gadget can be 3-colored such that output node of OR-gadget is colored True.

Reduction

- Create triangle with nodes True, False, Base.
- For each variable x_i two nodes v_i and \overline{v}_i connected in a triangle with common Base.
- For each clause $C_j = (a \lor b \lor c)$, add OR-gadget graph with input nodes a, b, c and connect output node of gadget to both False and Base.



Reduction

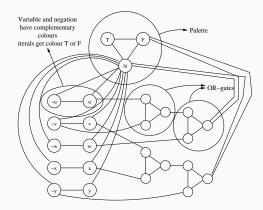


Lemma

No legal 3-coloring of above graph (with coloring of nodes T, F, B fixed) in which a, b, c are colored False. If any of a, b, c are colored True then there is a legal 3-coloring of above graph.

Reduction Outline

Example
$$\varphi = (u \lor \neg v \lor w) \land (v \lor x \lor \neg y)$$



• If x_i is assigned True, color v_i True and \overline{v}_i False.

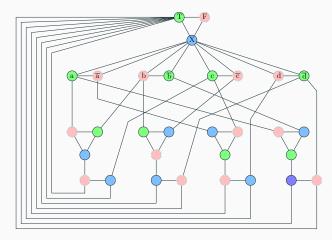
- If x_i is assigned True, color v_i True and \overline{v}_i False.
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- G_{φ} is 3-colorable implies φ is satisfiable
 - If *v_i* is colored True then set *x_i* to be True, this is a legal truth assignment.

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- G_{φ} is 3-colorable implies φ is satisfiable
 - If *v_i* is colored True then set *x_i* to be True, this is a legal truth assignment.
 - Consider any clause $C_j = (a \lor b \lor c)$. it cannot be that all a, b, c are False. If so, output of OR-gadget for C_j has to be colored False but output is connected to Base and False!

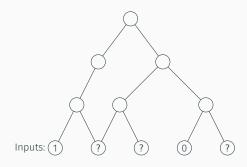
Graph generated in reduction from 3SAT to 3COLOR



Circuit-Sat Problem

Circuits

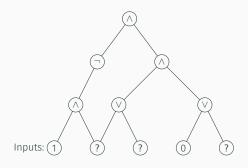
A circuit is a directed *acyclic* graph with



- Input vertices (without incoming edges) labeled with 0, 1 or a distinct variable.
- Every other vertex is labeled \lor , \land or \neg .
- Single node output vertex with no outgoing edges.

Circuits

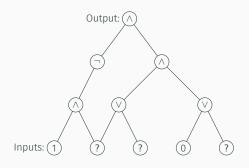
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Lemma CSAT is in NP.

- Certificate: Assignment to input variables.
- Certifier: Evaluate the value of each gate in a topological sort of DAG and check the output gate value.

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However they are equivalent in terms of polynomial-time solvability.

Theorem $SAT \leq_P 3SAT \leq_P CSAT$.

Theorem $CSAT \leq_P SAT \leq_P 3SAT.$

Given 3CNF formula φ with n variables and m clauses, create a Circuit C.

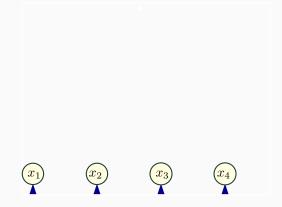
- Inputs to C are the *n* boolean variables x_1, x_2, \ldots, x_n
- Use NOT gate to generate literal $\neg x_i$ for each variable x_i
- + For each clause ($\ell_1 \lor \ell_2 \lor \ell_3$) use two OR gates to mimic formula
- Combine the outputs for the clauses using AND gates to obtain the final output

Example: 3SAT SAT

$$\varphi = \left(X_1 \lor \lor X_3 \lor X_4 \right) \land \left(X_1 \lor \neg X_2 \lor \neg X_3 \right) \land \left(\neg X_2 \lor \neg X_3 \lor X_4 \right)$$

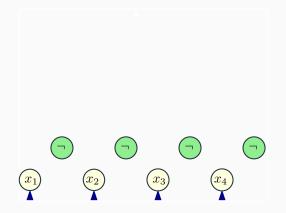
Example: $3SAT \leq_{P} CSAT$

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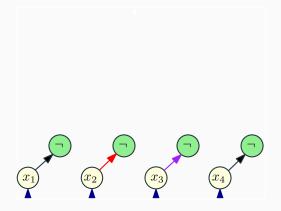
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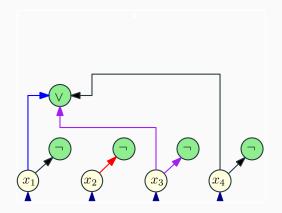
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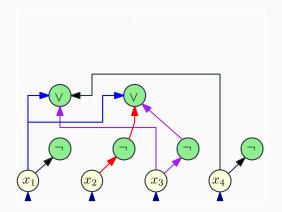
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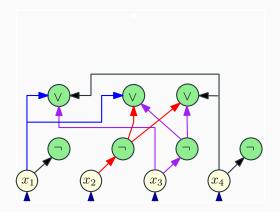


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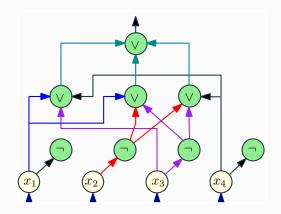


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$$\varphi = \left(X_1 \lor \lor X_3 \lor X_4 \right) \land \left(X_1 \lor \neg X_2 \lor \neg X_3 \right) \land \left(\neg X_2 \lor \neg X_3 \lor X_4 \right)$$



What will converting a circuit to a SAT formula prove?

Converting a circuit to a SAT formula

What will converting a circuit to a SAT formula prove?

But first we need to look back at a gadget!

Ζ	Х	у	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Ζ	Х	у	$z = x \wedge y$	
0	0	0	1	
0	0	1	1	
0	1	0	1	
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	0	
1	1	1	1	

Ζ	Х	у	$z = x \wedge y$				
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Ζ	Х	у	$z = x \wedge y$	$z \lor \overline{x} \ vee\overline{y}$			
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Ζ	Х	у	$z = x \wedge y$	$z \lor \overline{x} vee\overline{y}$	$\overline{z} \lor x \lor y$		
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Ζ	Х	у	$z = x \wedge y$	$z \lor \overline{x} \ vee\overline{y}$	$\overline{z} \lor x \lor y$	$\overline{z} \lor x \lor \overline{y}$	
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Ζ	Х	у	$z = x \wedge y$	$z \lor \overline{x} vee\overline{y}$	$\overline{z} \lor x \lor y$	$\overline{z} \lor x \lor \overline{y}$	$\overline{z} \lor \overline{x} \lor y$
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Ζ	Χ	у	$z = x \wedge y$	$z \lor \overline{x} \ vee\overline{y}$	$\overline{z} \lor x \lor y$	$\overline{z} \lor x \lor \overline{y}$	$\overline{z} \vee \overline{x} \vee y$
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

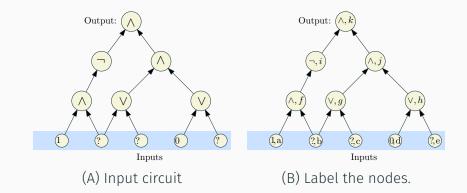
Ζ	Х	у	$z = x \wedge y$	$z \lor \overline{x} \ vee\overline{y}$	$\overline{z} \lor x \lor y$	$\overline{z} \lor x \lor \overline{y}$	$\overline{z} \vee \overline{x} \vee y$
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

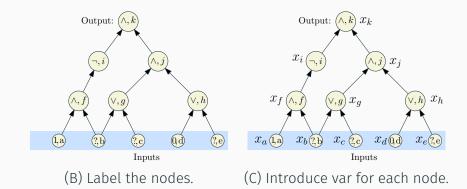
$$\left(z = x \land y \right)$$
$$\equiv$$

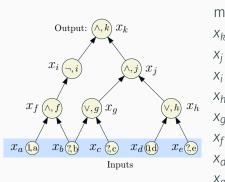
 $(z \lor \overline{x} \lor \overline{y}) \land (\overline{z} \lor x \lor y) \land (\overline{z} \lor x \lor \overline{y}) \land (\overline{z} \lor \overline{x} \lor y)$

Lemma The following identities hold:

$$\begin{array}{l} \cdot \ z = \overline{x} & \equiv & (z \lor x) \land (\overline{z} \lor \overline{x}) \, . \\ \cdot \ \left(z = x \lor y \right) & \equiv & (z \lor \overline{y}) \land (z \lor \overline{x}) \land (\overline{z} \lor x \lor y) \\ \cdot \ \left(z = x \land y \right) & \equiv & \left(z \lor \overline{x} \lor \overline{y} \right) \land \left(\overline{z} \lor x \right) \land \left(\overline{z} \lor y \right) \end{array}$$







$$x_{k} \text{ (Demand a sat' assign-ment!)}$$

$$x_{k} = x_{i} \land x_{j}$$

$$x_{j} = x_{g} \land x_{h}$$

$$x_{i} = \neg x_{f}$$

$$x_{h} = x_{d} \lor x_{e}$$

$$x_{g} = x_{b} \lor x_{c}$$

$$x_{f} = x_{a} \land x_{b}$$

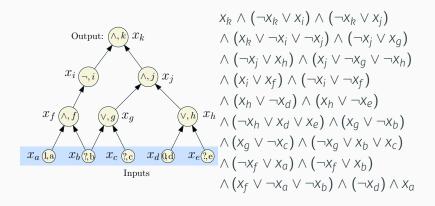
$$x_{d} = 0$$

$$x_{a} = 1$$

(C) Introduce var for each node.

(D) Write a sub-formula for each variable that is true if the var is computed correctly. 66

X _k	X _k
$x_k = x_i \wedge x_j$	$(\neg x_k \lor x_i) \land (\neg x_k \lor x_j) \land (x_k \lor \neg x_i \lor \neg x_j)$
$x_j = x_g \wedge x_h$	$(\neg x_j \lor x_g) \land (\neg x_j \lor x_h) \land (x_j \lor \neg x_g \lor \neg x_h)$
$X_i = \neg X_f$	$(x_i \lor x_f) \land (\neg x_i \lor \neg x_f)$
$X_h = X_d \vee X_e$	$(x_h \vee \neg x_d) \wedge (x_h \vee \neg x_e) \wedge (\neg x_h \vee x_d \vee x_e)$
$x_g = x_b \vee x_c$	$(x_g \vee \neg x_b) \land (x_g \vee \neg x_c) \land (\neg x_g \vee x_b \vee x_c)$
$X_f = X_a \wedge X_b$	$(\neg x_f \lor x_a) \land (\neg x_f \lor x_b) \land (x_f \lor \neg x_a \lor \neg x_b)$
$X_d = 0$	$\neg X_d$
$x_a = 1$	Xa



We got a CNF formula that is satisfiable if and only if the original circuit is satisfiable.

- For each gate (vertex) v in the circuit, create a variable x_v
- Case \neg : *v* is labeled \neg and has one incoming edge from *u* (so $x_v = \neg x_u$). In **SAT** formula generate, add clauses $(x_u \lor x_v)$, $(\neg x_u \lor \neg x_v)$. Observe that

$$x_v = \neg x_u$$
 is true $\iff (x_u \lor x_v) (\neg x_u \lor \neg x_v)$ both true.

Case ∨: So x_v = x_u ∨ x_w. In SAT formula generated, add clauses (x_v ∨ ¬x_u), (x_v ∨ ¬x_w), and (¬x_v ∨ x_u ∨ x_w). Again, observe that

$$\begin{pmatrix} x_v \lor \neg x_u \end{pmatrix}, \\ \begin{pmatrix} x_v \lor x_w \end{pmatrix} \text{ is true } \iff \begin{pmatrix} x_v \lor \neg x_u \end{pmatrix}, \\ \begin{pmatrix} x_v \lor \neg x_w \end{pmatrix}, \\ (\neg x_v \lor x_u \lor x_w) \end{pmatrix} \text{ all true.}$$

• Case \land : So $x_v = x_u \land x_w$. In SAT formula generated, add clauses $(\neg x_v \lor x_u)$, $(\neg x_v \lor x_w)$, and $(x_v \lor \neg x_u \lor \neg x_w)$. Again observe that

$$x_v = x_u \wedge x_w \text{ is true } \iff (\neg x_v \lor x_u), \\ (\neg x_v \lor x_w), \qquad \text{all true.} \\ (x_v \lor \neg x_u \lor \neg x_w)$$

- If v is an input gate with a fixed value then we do the following. If $x_v = 1$ add clause x_v . If $x_v = 0$ add clause $\neg x_v$
- Add the clause x_v where v is the variable for the output gate

Need to show circuit C is satisfiable iff φ_{C} is satisfiable

- \Rightarrow Consider a satisfying assignment *a* for *C*
 - Find values of all gates in C under a
 - Give value of gate v to variable x_v ; call this assignment a'
 - a' satisfies φ_{C} (exercise)
- \leftarrow Consider a satisfying assignment *a* for φ_C
 - Let a' be the restriction of a to only the input variables
 - Value of gate v under a' is the same as value of x_v in a
 - Thus, a' satisfies C