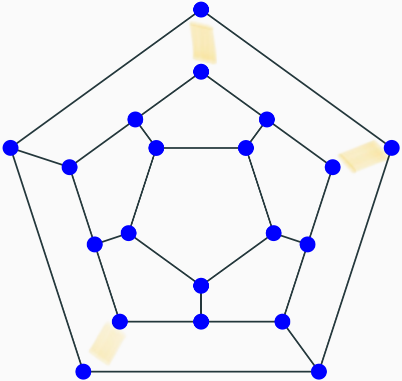
Pre-lecture brain teaser

Does this graph have a Hamiltonian cycle?



a Yes.

b No.

Answer: B. The outer cycle has two entrances/exits that aren't next to each other always leaving out one or two vertices.

ECE-374-B: Lecture 21 - Lots of NP-Complete reductions

Instructor: Abhishek Kumar Umrawal

November 9, 2022

University of Illinois at Urbana-Champaign

Today

NP-Completeness of the following two problems.

- Hamiltonian cycle
- 3-coloring

Important: Understanding the problems and that they are hard.

Proofs and reductions will be sketchy and mainly to give a flavor.

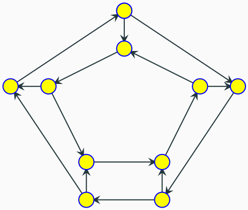
Reduction from 3SAT to Hamiltonian Cycle

Directed Hamiltonian Cycle

Input Given a directed graph $G = (V, E)$ with n vertices.

Goal Does G have a Hamiltonian cycle?

- A Hamiltonian cycle is a cycle in the graph that visits every vertex in G exactly once.



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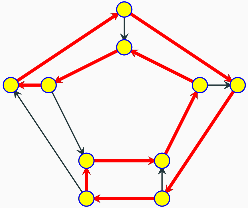
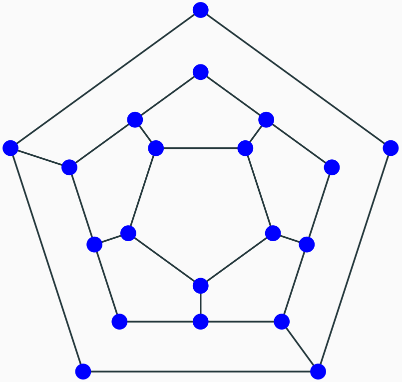


Is the following graph Hamiltonianan?



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Directed Hamiltonian Cycle is NP-Complete

(DHC)

- Directed Hamiltonian Cycle is in *NP*: exercise.
- Hardness: We will show the following.

3-SAT $\leq_P$ Directed Hamiltonian Cycle

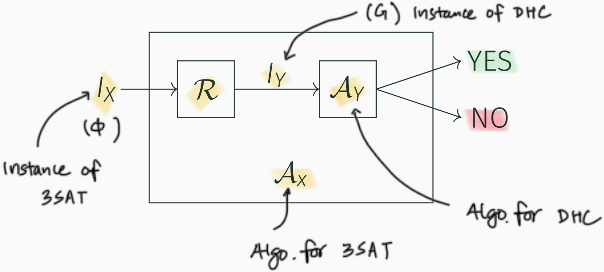
3SAT $\Rightarrow_P$ DHC

Directed Hamiltonian Cycle is NP-Complete

- Directed Hamiltonian Cycle is in *NP*: exercise.
- Hardness: We will show the following.

$$\underset{X}{\text{3-SAT}} \leq_P \underset{Y}{\text{Directed Hamiltonian Cycle}} \text{ (DHC)}$$

We have the following reduction diagram.



Reduction

Given 3-SAT formula φ create a graph G_φ such that the following hold.

- G_φ has a Hamiltonian cycle if and only if φ is satisfiable.
- G_φ should be constructible from φ by a polynomial time algorithm $\mathcal{A}$.

Notation: φ has n variables $x_1, x_2, \ldots, x_n$ and m clauses $C_1, C_2, \ldots, C_m$.

Reduction: First Ideas

- Viewing SAT: Assign values to n variables, and each clauses has 3 ways in which it can be satisfied.
- Construct graph with 2^n Hamiltonian cycles, where each cycle corresponds to some boolean assignment.
- Then add more graph structure to encode constraints on assignments imposed by the clauses.

Reduction: Encoding idea I

Need to create a graph from any arbitrary boolean assignment. Consider the following expression.

$$f(x_1) = 1 \tag{1}$$

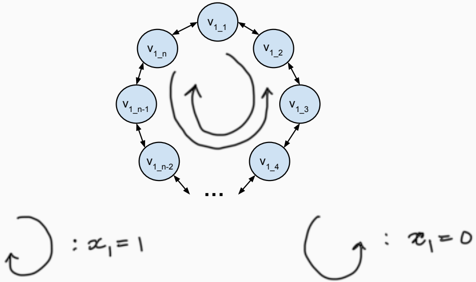
x_1	$f(x_1)$
1	1
0	1

Reduction: Encoding idea I

Need to create a graph from any arbitrary boolean assignment. Consider the following expression.

$$f(x_1) = 1 \quad (1)$$

We create a cyclic graph that always has a Hamiltonian cycle.



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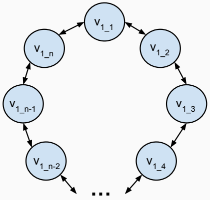


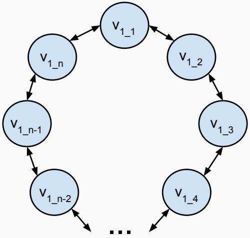
But how do we encode the variable?

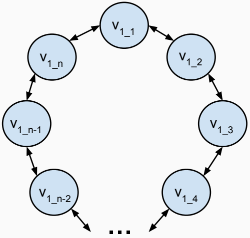
Reduction: Encoding idea I

Need to create a graph from any arbitrary boolean assignment. Consider the following expression.

$$f(x_1) = 1$$

Maybe we can encode the variable x_1 in terms of the cycle direction.





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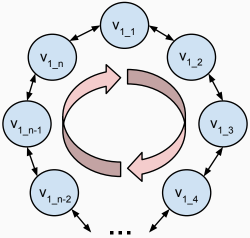
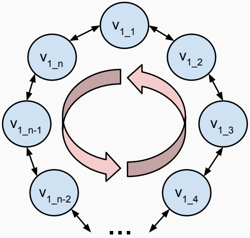


If $x_1 = 1$



If $x_1 = 0$

Reduction: Encoding idea II

How do we encode multiple variables?

$$f(x_1, x_2) = 1 \tag{2}$$

Maybe two circles? Now we need to connect them so that we have a single Hamiltonian cycle.

x_1	x_2	$f(x_1, x_2)$
1	0	1
0	1	1
0	0	1
1	1	1

Reduction: Encoding idea II

How do we encode multiple variables?

$$f(x_1, x_2) = 1 \tag{2}$$

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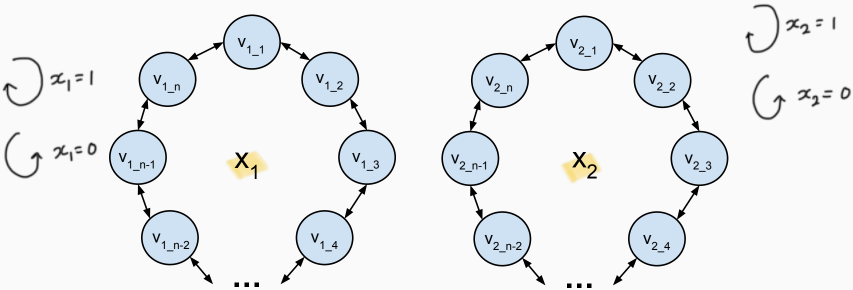
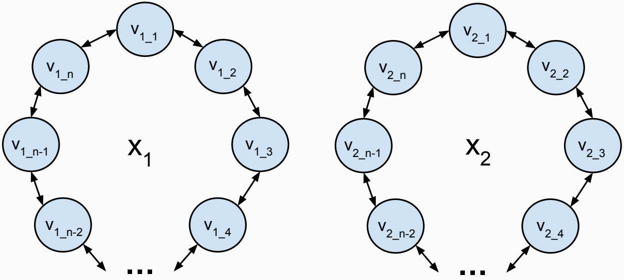


Reduction: Encoding idea II

How do we encode multiple variables?

$$f(x_1, x_2) = 1 \tag{3}$$

Now we need to connect them so that we have a single Hamiltonian path



Reduction: Encoding idea II

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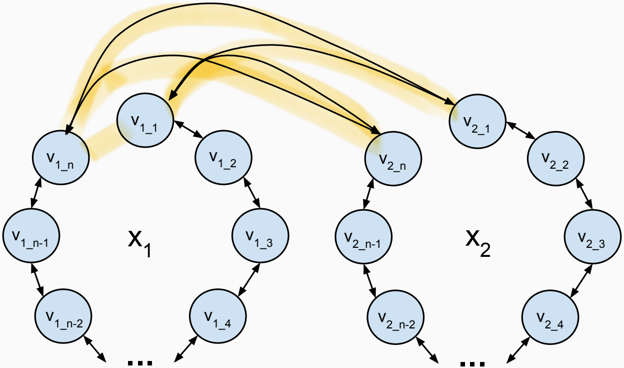
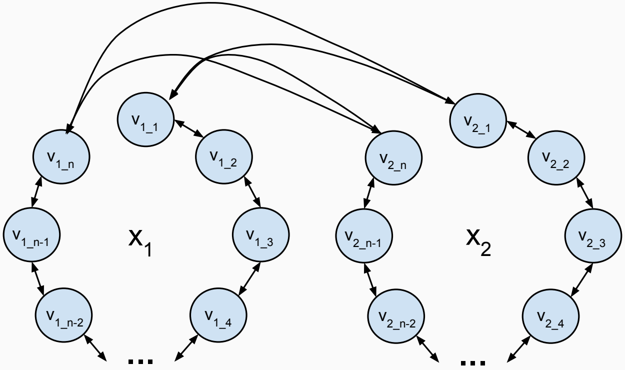


How do we encode multiple variables?

$$f(x_1, x_2) = 1 \tag{4}$$

Would be nice to have a single start/stop node.



Reduction: Encoding idea II

How do we encode multiple variables?

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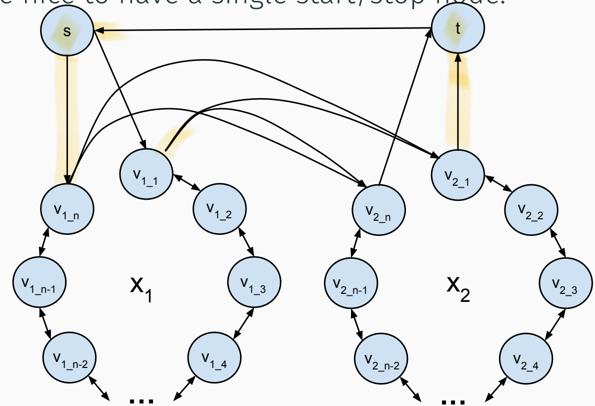
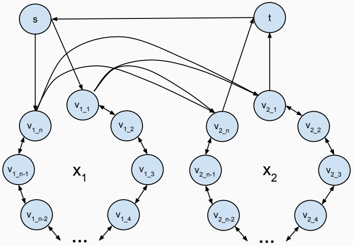


Reduction: Encoding idea II

How do we encode multiple variables?

$$f(x_1, x_2) = 1 \tag{5}$$

Getting a bit messy. Let's reorganize as follows.

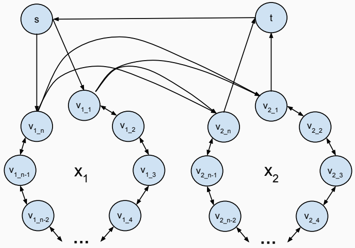


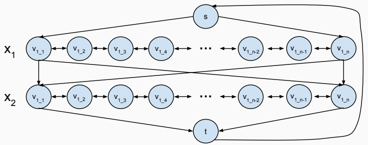
Reduction: Encoding idea II

How do we encode multiple variables?

$$f(x_1, x_2) = 1 \quad (5)$$

Getting a bit messy. Let's reorganize as follows.



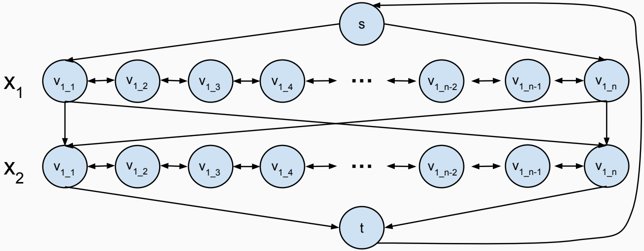


Reduction: Encoding idea II

How do we encode multiple variables?

$$f(x_1, x_2) = 1 \tag{6}$$

This is how we encode variable assignments in a variable loop!

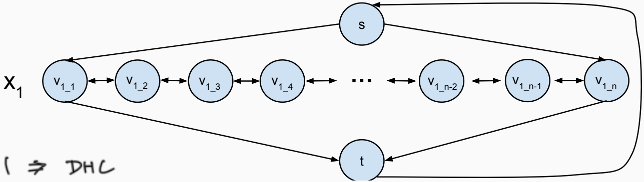


How do we handle clauses?

$$f(x_1) = x_1 \tag{7}$$

Lets go back to our one variable graph.

x_1	$f(x_1)$
1	1
0	0



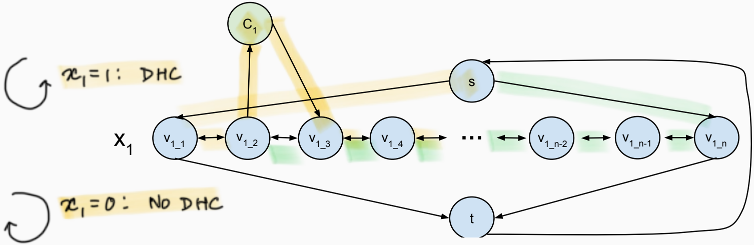
$x_1 = 1 \Rightarrow$ DHC

$x_1 = 0 \Rightarrow$ NO DHC

How do we handle clauses?

$$f(x_1) = x_1 \tag{8}$$

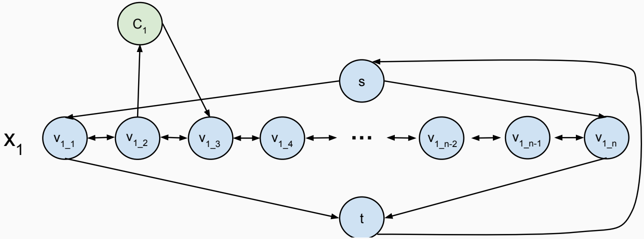
Add node for clause.



How do we handle clauses?

$$f(x_1, x_2) = (x_1 \vee \overline{x_2}) \quad (9)$$

What do we do if the clause has two literals?



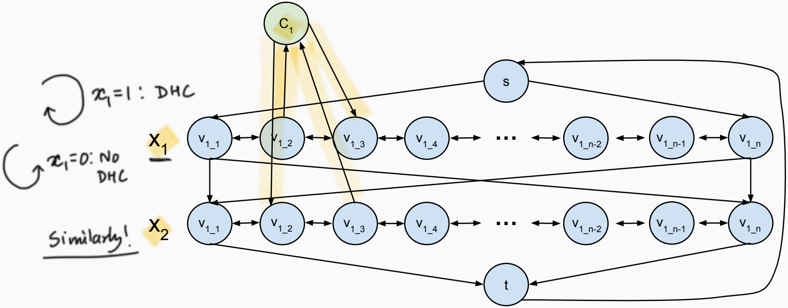
Reduction: Encoding idea III

How do we handle clauses?

$$f(x_1, x_2) = (x_1 \vee \overline{x_2}) \tag{9}$$

x_1	x_2	$f(x_1, x_2)$
1	0	
0	1	
0	0	
1	1	

What do we do if the clause has two literals?

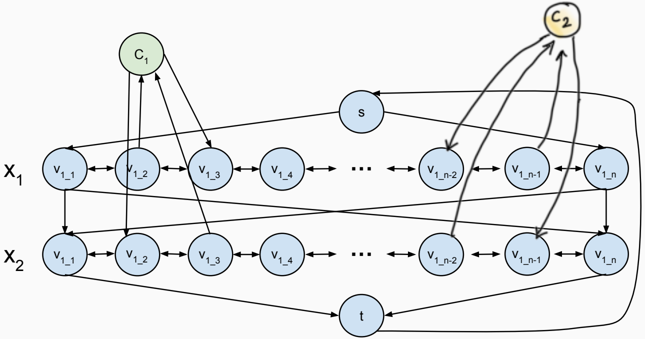


Reduction: Encoding idea III

How do we handle clauses?

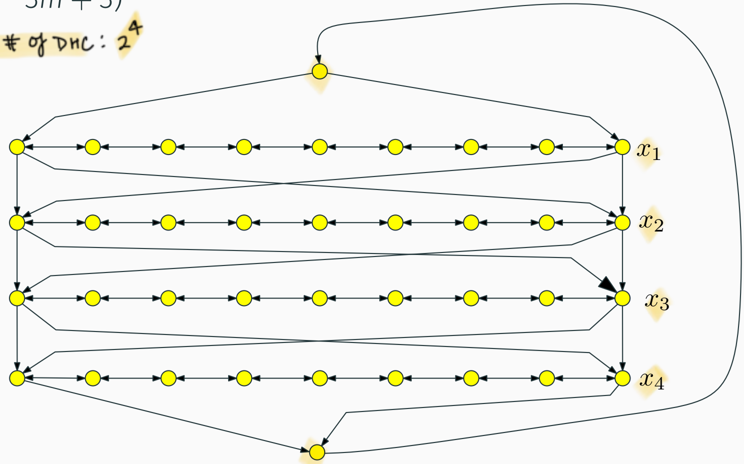
$$f(x_1, x_2) = (x_1 \vee \overline{x_2}) \wedge (\overline{x_1} \vee x_2) \tag{10}$$

What if the expression has multiple clauses:



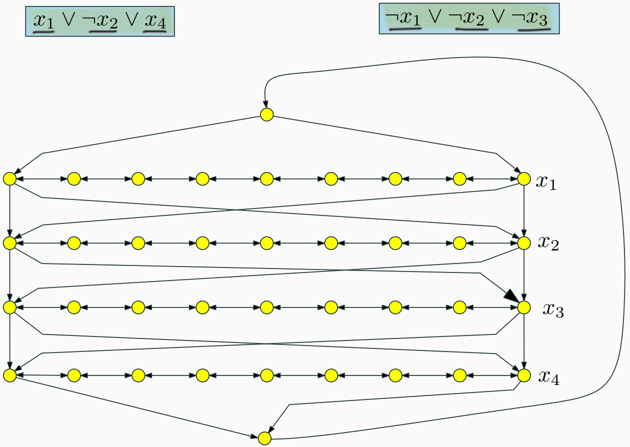
- Traverse path i from left to right iff x_i is set to true
- Each path has $3(m+1)$ nodes where m is number of clauses in φ; nodes numbered from left to right (1 to $3m+3$)

Exhaustive # of DHC : 2^4



The Reduction algorithm: Review II

Add vertex c_j for clause C_j. c_j has edge *from* vertex $3j$ and *to* vertex $3j+1$ on path i if x_i appears in clause C_j, and has edge *from* vertex $3j+1$ and *to* vertex $3j$ if $\neg x_i$ appears in C_j.



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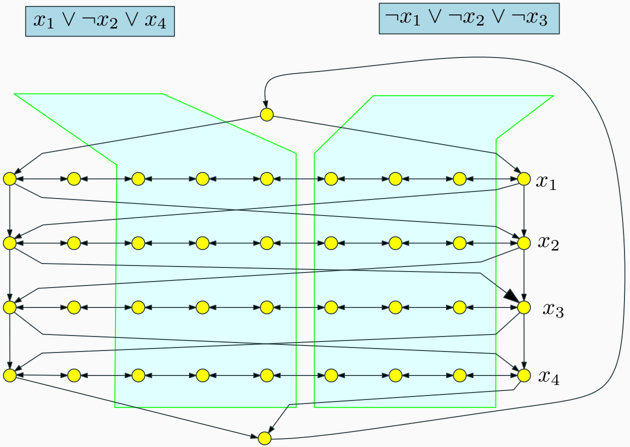

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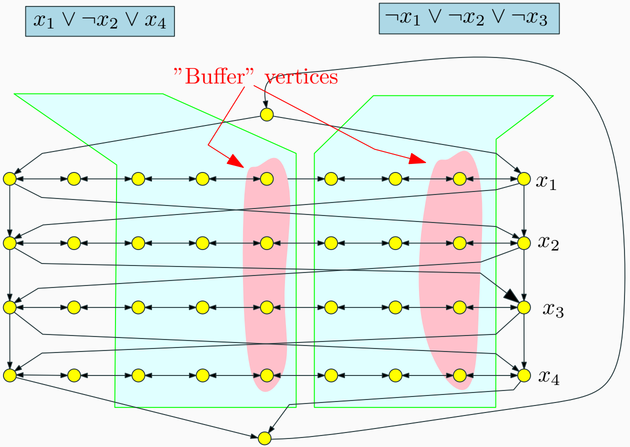

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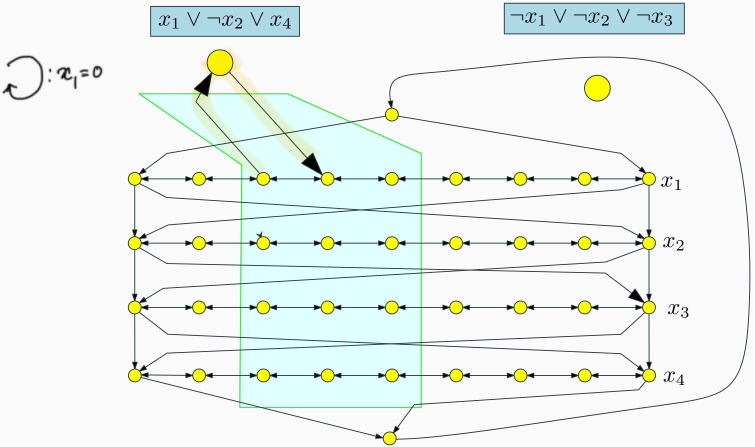

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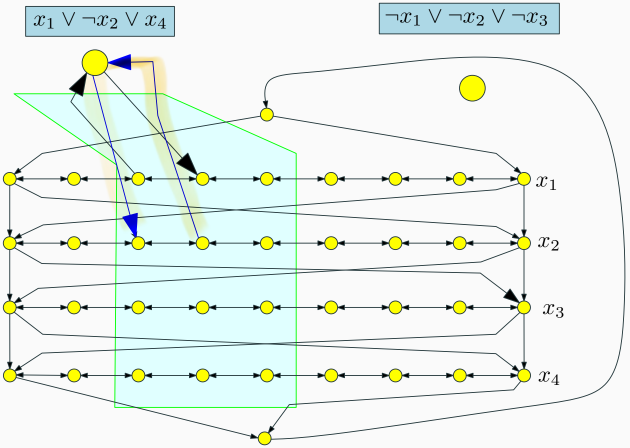

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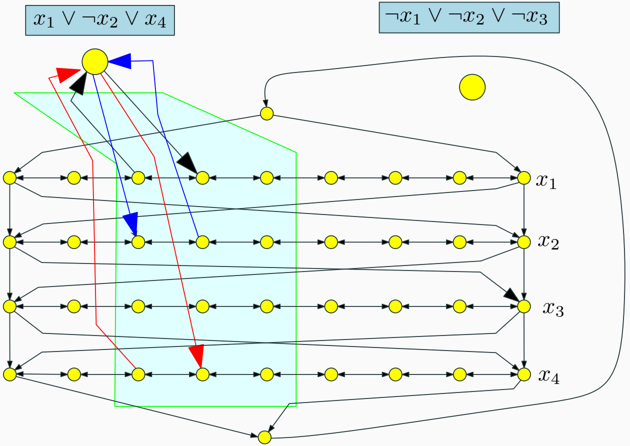

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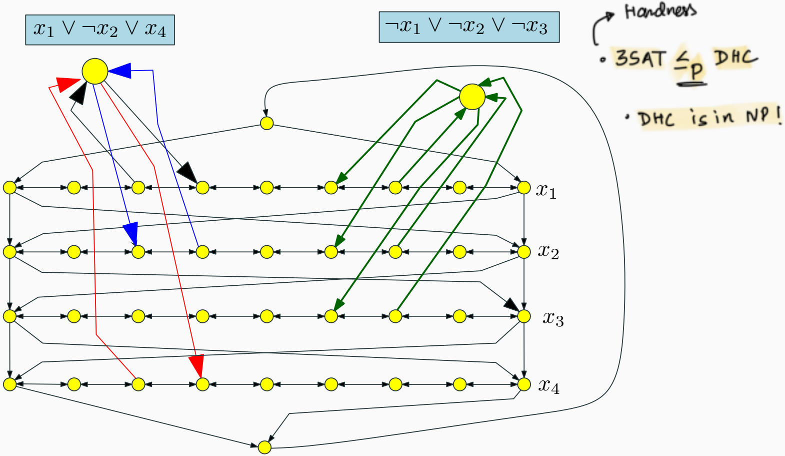

Correctness Proof (RIY)

Theorem
φ has a satisfying assignment iff G_φ has a Hamiltonian cycle.

Based on proving the following two lemmas.

Lemma
If φ has a satisfying assignment then G_φ has a Hamilton cycle.

Lemma
If G_φ has a Hamilton cycle then φ has a satisfying assignment.

Satisfying assignment $\rightarrow$ Hamiltonian Cycle

Lemma
If φ has a satisfying assignment then G_φ has a Hamilton cycle.

Proof.

$\Rightarrow$ Let a be the satisfying assignment for φ. Define Hamiltonian cycle as follows.

- If $a(x_i) = 1$ then traverse path i from left to right.
- If $a(x_i) = 0$ then traverse path i from right to left.
- For each clause, path of at least one variable is in the "right" direction to splice in the node corresponding to clause. $\square$

Suppose Π is a Hamiltonian cycle in G_φ.

Definition
We say Π is *canonical* if for each clause vertex c_j the edge of Π entering c_j and edge of Π leaving c_j are from the same path corresponding to some variable x_i. Otherwise Π is *non-canonical* or emphcheating.

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Lemma
Every Hamilton cycle in G_φ is canonical.

Proof of Lemma

Lemma
Every Hamilton cycle in G_φ is canonical.

- If Π enters c_j (vertex for clause C_j) from vertex $3j$ on path i then it must leave the clause vertex on edge to $3j+1$ on the *same path* i.
  - If not, then only unvisited neighbor of $3j+1$ on path i is $3j+2$.
  - Thus, we don't have two unvisited neighbors (one to enter from, and the other to leave) to have a Hamiltonian Cycle.
- Similarly, if Π enters c_j from vertex $3j+1$ on path i then it must leave the clause vertex c_j on edge to $3j$ on path i.

Hamiltonian Cycle $\implies$ Satisfying assignment (contd)

Lemma
Any canonical Hamilton cycle in G_φ corresponds to a satisfying truth assignment to φ.

Consider a canonical Hamilton cycle Π.

- For every clause vertex c_j, vertices visited immediately before and after c_j are connected by an edge on same path corresponding to some variable x_i.
- We can remove c_j from cycle, and get Hamiltonian cycle in $G - c_j$.
- Hamiltonian cycle from Π in $G - \{c_1, \ldots c_m\}$ traverses each path in only one direction, which determines truth assignment.
- Easy to verify that this truth assignment satisfies φ.

Hamiltonian cycle in undirected graph

Hamiltonian Cycle in *Undirected* Graphs

Problem

Input *Given undirected graph* $G = (V, E)$.

Goal *Does G have a Hamiltonian cycle? That is, is there a cycle that visits every vertex exactly one (except start and end vertex)?*

Theorem (UHC)

Hamiltonian cycle problem for undirected graphs is NP-Complete.

Proof.

- The problem is in **NP**; proof left as exercise.
- Hardness proved by reducing Directed Hamiltonian Cycle to this problem. □

We want to do now!

$3SAT \leq_P DHC \leq_P UHC$

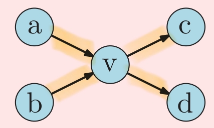
Already done!

Reduction Sketch

Goal: Given directed graph G, need to construct undirected graph G' such that G has Hamiltonian cycle iff G' has Hamiltonian ~~path~~ cycle.

Reduction

-
-

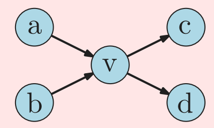


Reduction Sketch

Goal: Given directed graph G, need to construct undirected graph G' such that G has Hamiltonian cycle iff G' has Hamiltonian path.

Reduction

- Replace each vertex v by 3 vertices: v_{in}, v, and v_{out}.
-

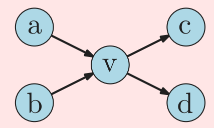


Reduction Sketch

Goal: Given directed graph G, need to construct undirected graph G' such that G has Hamiltonian cycle iff G' has Hamiltonian path.

Reduction

- Replace each vertex v by 3 vertices: v_{in}, v, and v_{out}.
- A directed edge (a, b) is replaced by edge (a_{out}, b_{in}).



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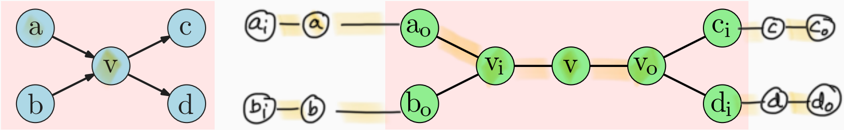
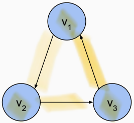
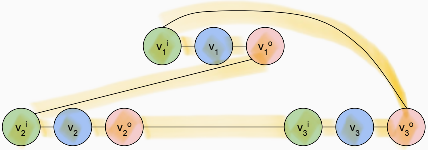


Reduction Sketch Example

Graph *with* cycle:





3 nodes

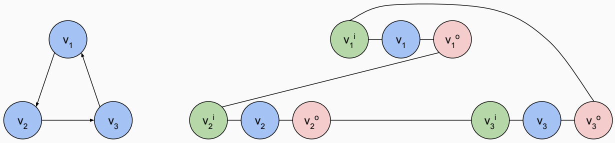
3 edges

$3 \cdot 3$ nodes : 9 nodes

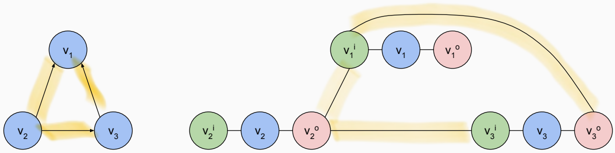
$(2 \cdot 3) + 3$ edges : 9 edges

Reduction Sketch Example

Graph *with* cycle:



Graph *without* cycle:



Reduction: Wrapup

- The reduction is polynomial time: exercise.
- The reduction is correct: exercise.

Hamiltonian Path

Input Given a graph $G = (V, E)$ with n vertices

Goal Does G have a Hamiltonian path?

- A Hamiltonian path is a path in the graph that visits every vertex in G exactly once.

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(TRY!)

Easy to modify the reduction from **3-SAT** to **Halitonian Cycle** or do a reduction from **Halitonian Cycle**.

Implies that **Longest Simple Path** in a graph is NP-Complete.

NP-Completeness of Graph Coloring

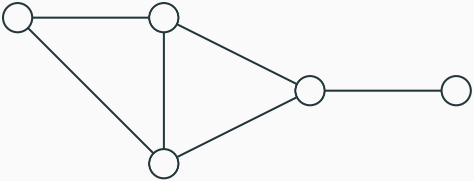
Problem: Graph Coloring

Instance: $G = (V, E)$: Undirected graph, integer k.
Question: Can the vertices of the graph be colored using k colors so that vertices connected by an edge do not get the same color?

Graph 3-Coloring

Problem: 3 Coloring

Instance: $G = (V, E)$: Undirected graph.
Question: Can the vertices of the graph be colored using 3 colors so that vertices connected by an edge do not get the same color?



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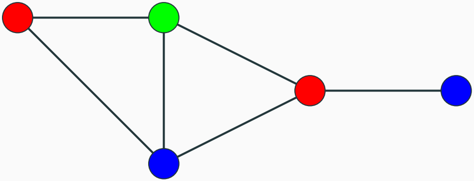

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Graph Coloring

Observation: If G is colored with k colors then each color class (nodes of same color) form an independent set in G. Thus, G can be partitioned into k independent sets iff G is k-colorable.

Graph 2-Coloring can be decided in polynomial time.

G is 2-colorable iff G is bipartite! There is a linear time algorithm to check if G is bipartite using breadth first search.

Problems related to graph coloring (RIY)

Register Allocation
Assign variables to (at most) k registers such that variables needed at the same time are not assigned to the same register.

Interference Graph
Vertices are variables, and there is an edge between two vertices, if the two variables are "live" at the same time.

Observations

- [Chaitin] Register allocation problem is equivalent to coloring the interference graph with k colors.
- Moreover, 3-COLOR $\leq_P$ k − Register Allocation, for any $k \geq 3$.

Class Room Scheduling

Given n classes and their meeting times, are k rooms sufficient?

Reduce to Graph k-Coloring problem.

Create graph G

- a node v_i for each class i.
- an edge between v_i and v_j if classes i and j *conflict*.

Exercise: G is k-colorable iff k rooms are sufficient.

Frequency Assignments in Cellular Networks

Cellular telephone systems that use Frequency Division Multiple Access (FDMA) (example: GSM in Europe and Asia and AT&T in USA).

- Breakup a frequency range $[a, b]$ into disjoint *bands* of frequencies $[a_0, b_0], [a_1, b_1], \ldots, [a_k, b_k]$.
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- Constraint: nearby towers cannot be assigned same band, otherwise signals will interference.

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- Each cell phone tower (simplifying) gets one band.
- Constraint: nearby towers cannot be assigned same band, otherwise signals will interference.

Problem: given k bands and some region with n towers, is there a way to assign the bands to avoid interference?

Can reduce to k-coloring by creating interference/conflict graph on towers.

Showing hardness of 3 COLORING

3-Coloring is NP-Complete

- 3-Coloring is in NP.
  - Non-deterministically guess a 3-coloring for each node
  - Check if for each edge (u, v), the color of u is different from that of v. (Exercise!)
- Hardness: We will show 3-SAT $\leq_P$ 3-Coloring.

Reduction Idea

Start with 3SAT formula (i.e., 3CNF formula) φ with n variables $x_1, \ldots, x_n$ and m clauses $C_1, \ldots, C_m$. Create graph G_φ such that G_φ is 3-colorable iff φ is satisfiable.

- need to establish truth assignment for $x_1, \ldots, x_n$ via colors for some nodes in G_φ.
- create triangle with node True, False, Base.
- for each variable x_i two nodes v_i and $\bar{v}_i$ connected in a triangle with common Base.
- If graph is 3-colored, either v_i or $\bar{v}_i$ gets the same color as True. Interpret this as a truth assignment to v_i.
- Need to add constraints to ensure clauses are satisfied (next phase).

Reduction Idea I - Simple 3-color gadget

We want to create a gadget that:

- Is 3 colorable if at least one of the literals is true.
- Not 3-colorable if none of the literals are true.

$\phi : C_1 \wedge C_2 \wedge \cdots \wedge C_m$

↳ E.g.: $C_1 = x_1 \vee x_2 \vee x_3$

↳ True if at least one of the literals is True!

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$$f(x_1, x_2) = (x_1 \vee x_2) \tag{11}$$

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Let's try some stuff:

Reduction Idea I - Simple 3-color gadget

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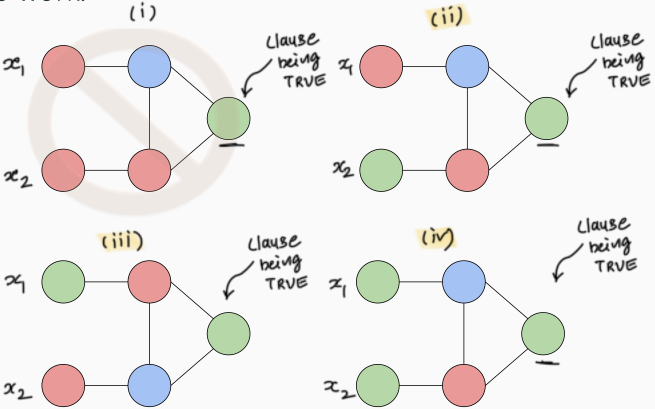
- Not 3-colorable if none of the literals are true

Seems to work:



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How do we do the same thing for 3 variables?

$$f(x_1, x_2, x_3) = (x_1 \vee x_2 \vee x_3) \tag{12}$$

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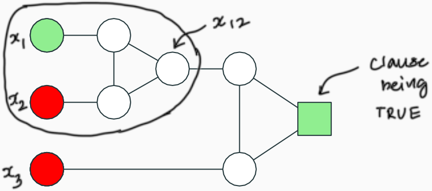
Assume green=true and red=false.

3 color this gadget II

You are given three colors: red, green and blue. Can the following graph be three colored in a valid way (assuming that some of the nodes are already colored as indicated).

$x_1 \vee x_2 \vee x_3$

$x_{12} \vee x_3$



a Yes.

b No.

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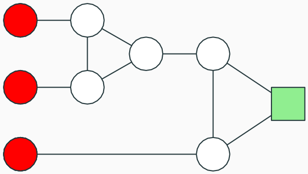
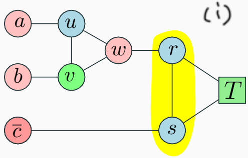


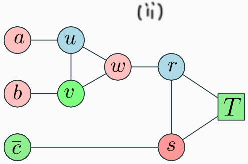
a Yes.

b No.

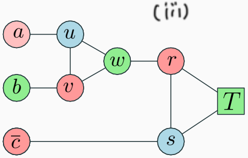
3-coloring of the clause gadget



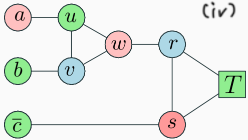
FFF - BAD



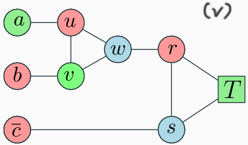
FFT



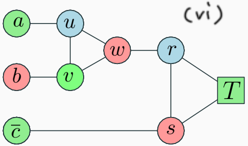
FTF



FTT



TFF



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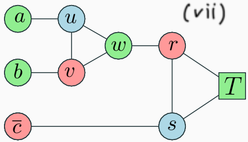

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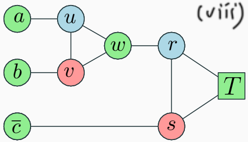


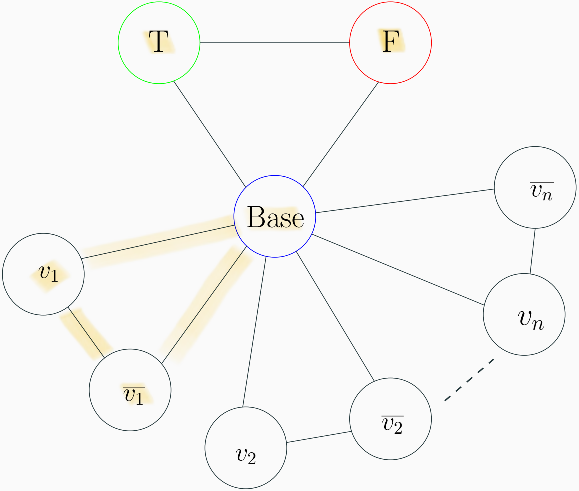
TTT

Reduction Idea II - Literal Assignment I

Next we need a gadget that assigns literals. Our previously constructed gadget assumes the following.

- All literals are either red or green.
- Need to limit graph so only x_1 or $\overline{x_1}$ is green. Other must be red.

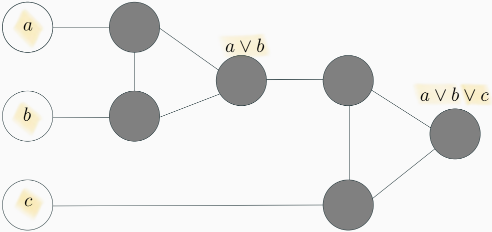
Reduction Idea II - Literal Assignment II



For each clause $C_j = (a \vee b \vee c)$, create a small gadget. graph

- Gadget graph connects to nodes corresponding to a, b, c.
- Needs to implement OR.

OR-gadget-graph:



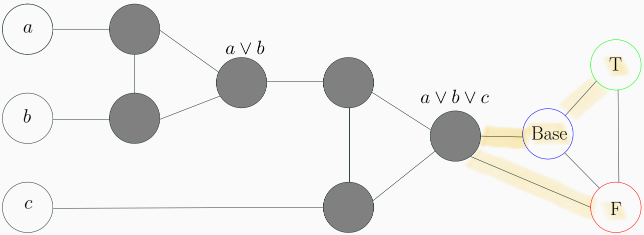
OR-Gadget Graph

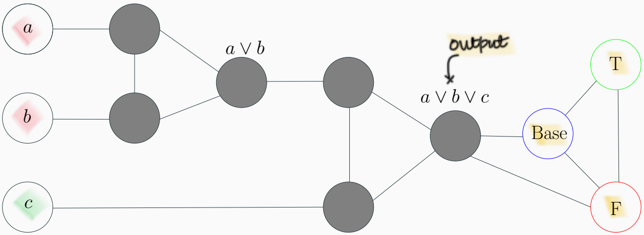
Property: If a, b, c are colored False in a 3-coloring then output node of OR-gadget has to be colored False.

Property: If one of a, b, c is colored True then OR-gadget can be 3-colored such that output node of OR-gadget is colored True.

Reduction

- Create triangle with nodes True, False, Base.
- For each variable x_i two nodes v_i and $\bar{v}_i$ connected in a triangle with common Base.
- For each clause $C_j = (a \vee b \vee c)$, add OR-gadget graph with input nodes a, b, c and connect output node of gadget to both False and Base.





Lemma

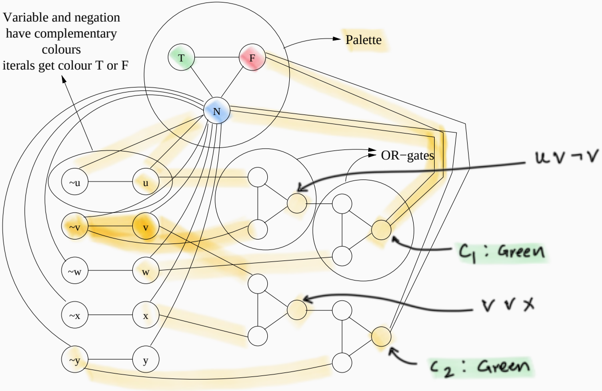
No legal 3-coloring of above graph (with coloring of nodes T, F, B fixed) in which a, b, c are colored False. If any of a, b, c are colored True then there is a legal 3-coloring of above graph.

Example

$\varphi = (u \vee \neg v \vee w) \wedge (v \vee x \vee \neg y)$

C_1 C_2

u
v
w
x
y



Correctness of Reduction (RIY)

φ is satisfiable implies G_φ is 3-colorable

- If x_i is assigned True, color v_i True and $\bar{v}_i$ False.

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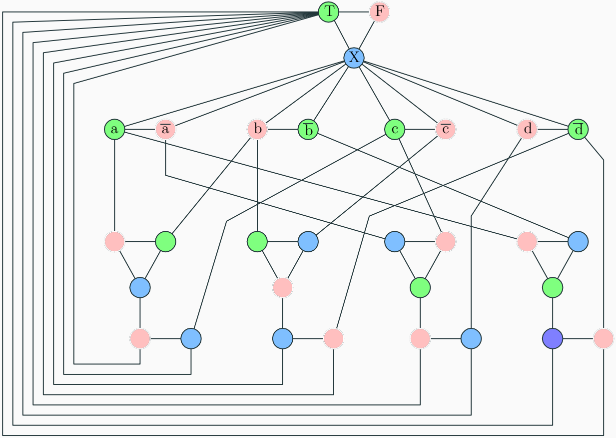
G_φ is 3-colorable implies φ is satisfiable

- If v_i is colored True then set x_i to be True, this is a legal truth assignment.
- Consider any clause $C_j = (a \vee b \vee c)$. it cannot be that all a, b, c are False. If so, output of OR-gadget for C_j has to be colored False but output is connected to Base and False!

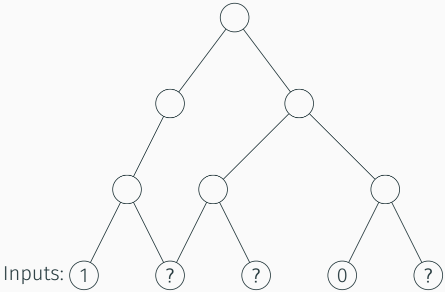
Graph generated in reduction from 3SAT to 3COLOR



Circuit-Sat Problem

Circuits

A circuit is a directed *acyclic* graph with



- Input vertices (without incoming edges) labeled with 0, 1 or a distinct variable.
- Every other vertex is labeled $\vee$, $\wedge$ or $\neg$.
- Single node output vertex with no outgoing edges.

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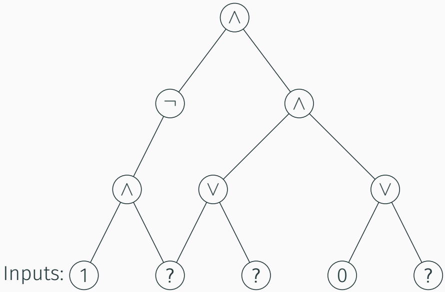

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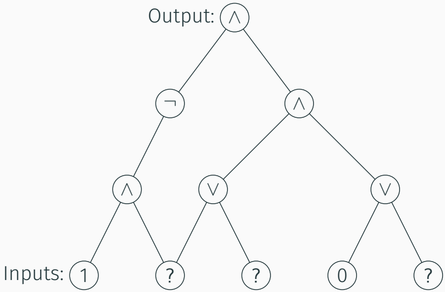

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CSAT: Circuit Satisfaction

Definition (Circuit Satisfaction (CSAT).)
Given a circuit as input, is there an assignment to the input variables that causes the output to get value 1?

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Given a circuit as input, is there an assignment to the input variables that causes the output to get value 1?

Lemma
CSAT is in NP.

- Certificate: Assignment to input variables.
- Certifier: Evaluate the value of each gate in a topological sort of DAG and check the output gate value.

Circuit SAT vs SAT

CNF formulas are a rather restricted form of Boolean formulas.

Circuits are a much more powerful (and hence easier) way to express Boolean formulas

Circuit SAT vs SAT

CNF formulas are a rather restricted form of Boolean formulas.

Circuits are a much more powerful (and hence easier) way to express Boolean formulas

However they are equivalent in terms of polynomial-time solvability.

Theorem
SAT $\leq_P$ *3SAT* $\leq_P$ *CSAT*.

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CSAT $\leq_P$ *SAT* $\leq_P$ *3SAT*.

Converting a CNF formula into a Circuit

Given 3CNF formula φ with n variables and m clauses, create a Circuit C.

- Inputs to C are the n boolean variables $x_1, x_2, \ldots, x_n$
- Use NOT gate to generate literal $\neg x_i$ for each variable x_i
- For each clause $(\ell_1 \vee \ell_2 \vee \ell_3)$ use two OR gates to mimic formula
- Combine the outputs for the clauses using AND gates to obtain the final output

Example: 3SAT $\leq_P$ CSAT

$$\varphi = \left(x_1 \vee \vee x_3 \vee x_4\right) \wedge \left(x_1 \vee \neg x_2 \vee \neg x_3\right) \wedge \left(\neg x_2 \vee \neg x_3 \vee x_4\right)$$

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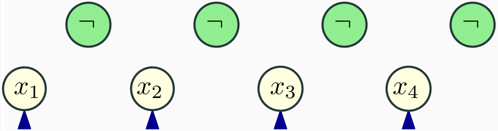

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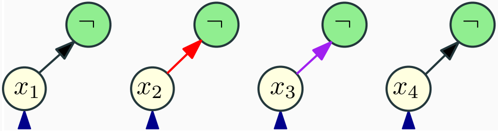

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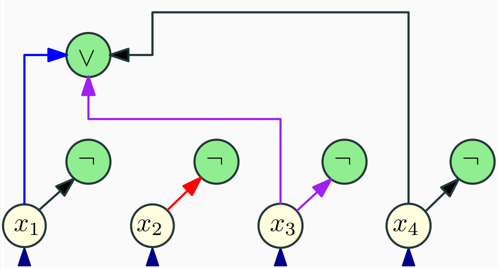

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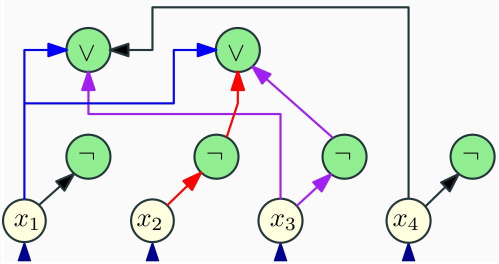

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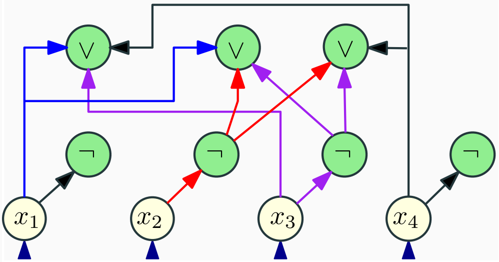

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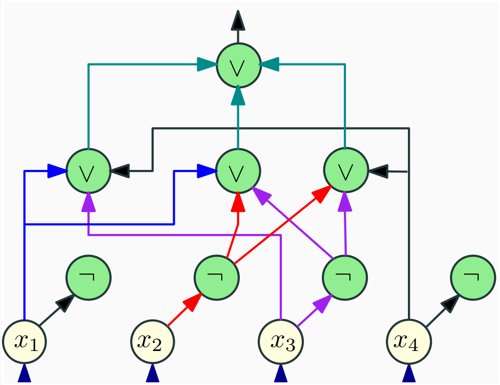


Converting a circuit to a SAT formula

What will converting a circuit to a SAT formula prove?

Converting a circuit to a SAT formula

What will converting a circuit to a SAT formula prove?

But first we need to look back at a gadget!

Converting $z = x \wedge y$ to 3SAT

z	x	y					
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$				
0	0	0	1				
0	0	1	1				
0	1	0	1				
0	1	1	0				
1	0	0	0				
1	0	1	0				
1	1	0	0				
1	1	1	1				

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$				
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$	$z \vee \overline{x}$ $vee\overline{y}$			
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$	$z \vee \overline{x}$ $vee\overline{y}$	$\overline{z} \vee x \vee y$		
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$	$z \vee \bar{x}\ vee \bar{y}$	$\bar{z} \vee x \vee y$	$\bar{z} \vee x \vee \bar{y}$	
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$	$z \vee \bar{x}\ vee\bar{y}$	$\bar{z} \vee x \vee y$	$\bar{z} \vee x \vee \bar{y}$	$\bar{z} \vee \bar{x} \vee y$
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$	$z \vee \bar{x}$ $vee\bar{y}$	$\bar{z} \vee x \vee y$	$\bar{z} \vee x \vee \bar{y}$	$\bar{z} \vee \bar{x} \vee y$
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

Converting $z = x \wedge y$ to 3SAT

z	x	y	$z = x \wedge y$	$z \vee \bar{x}$ $vee\bar{y}$	$\bar{z} \vee x \vee y$	$\bar{z} \vee x \vee \bar{y}$	$\bar{z} \vee \bar{x} \vee y$
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1

$$\Big(z = x \wedge y\Big)$$

$$\equiv$$

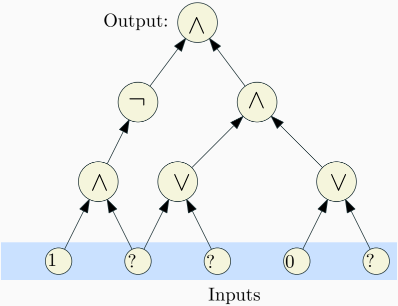
$$(z \vee \bar{x} \vee \bar{y}) \wedge (\bar{z} \vee x \vee y) \wedge (\bar{z} \vee x \vee \bar{y}) \wedge (\bar{z} \vee \bar{x} \vee y)$$

Summary of formulas we derived

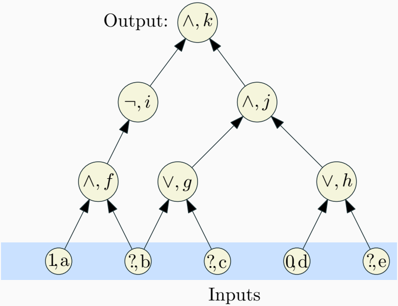
Lemma
The following identities hold:

- $z = \bar{x} \quad \equiv \quad (z \vee x) \wedge (\bar{z} \vee \bar{x})\,.$
- $\left(z = x \vee y\right) \quad \equiv \quad (z \vee \bar{y}) \wedge (z \vee \bar{x}) \wedge (\bar{z} \vee x \vee y)$
- $\left(z = x \wedge y\right) \quad \equiv \quad \left(z \vee \bar{x} \vee \bar{y}\right) \wedge \left(\bar{z} \vee x\right) \wedge \left(\bar{z} \vee y\right)$

Converting a circuit into a CNF formula

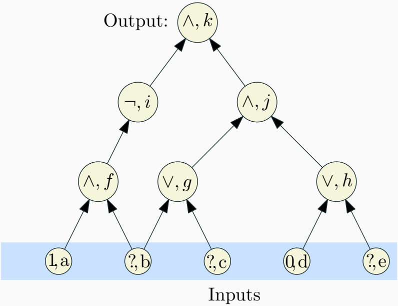


(A) Input circuit

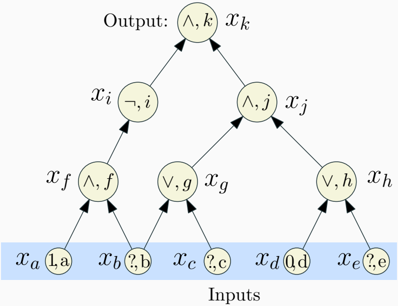


(B) Label the nodes.

Converting a circuit into a CNF formula

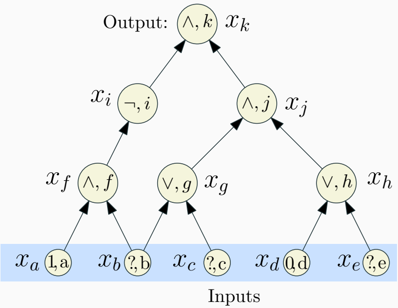


(B) Label the nodes.



(C) Introduce var for each node.

Converting a circuit into a CNF formula



(C) Introduce var for each node.

x_k (Demand a sat' assignment!)

$x_k = x_i \wedge x_j$

$x_j = x_g \wedge x_h$

$x_i = \neg x_f$

$x_h = x_d \vee x_e$

$x_g = x_b \vee x_c$

$x_f = x_a \wedge x_b$

$x_d = 0$

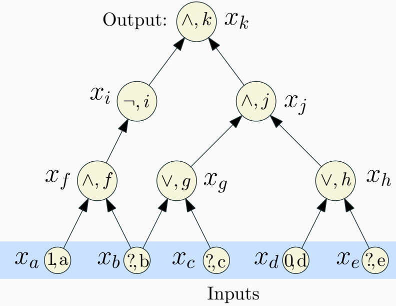
$x_a = 1$

(D) Write a sub-formula for each variable that is true if the var is computed correctly.

Converting a circuit into a CNF formula

x_k	x_k
$x_k = x_i \wedge x_j$	$(\neg x_k \vee x_i) \wedge (\neg x_k \vee x_j) \wedge (x_k \vee \neg x_i \vee \neg x_j)$
$x_j = x_g \wedge x_h$	$(\neg x_j \vee x_g) \wedge (\neg x_j \vee x_h) \wedge (x_j \vee \neg x_g \vee \neg x_h)$
$x_i = \neg x_f$	$(x_i \vee x_f) \wedge (\neg x_i \vee \neg x_f)$
$x_h = x_d \vee x_e$	$(x_h \vee \neg x_d) \wedge (x_h \vee \neg x_e) \wedge (\neg x_h \vee x_d \vee x_e)$
$x_g = x_b \vee x_c$	$(x_g \vee \neg x_b) \wedge (x_g \vee \neg x_c) \wedge (\neg x_g \vee x_b \vee x_c)$
$x_f = x_a \wedge x_b$	$(\neg x_f \vee x_a) \wedge (\neg x_f \vee x_b) \wedge (x_f \vee \neg x_a \vee \neg x_b)$
$x_d = 0$	$\neg x_d$
$x_a = 1$	x_a

Converting a circuit into a CNF formula



$$
\begin{aligned}
& x_k \wedge (\neg x_k \vee x_i) \wedge (\neg x_k \vee x_j) \\
& \wedge (x_k \vee \neg x_i \vee \neg x_j) \wedge (\neg x_j \vee x_g) \\
& \wedge (\neg x_j \vee x_h) \wedge (x_j \vee \neg x_g \vee \neg x_h) \\
& \wedge (x_i \vee x_f) \wedge (\neg x_i \vee \neg x_f) \\
& \wedge (x_h \vee \neg x_d) \wedge (x_h \vee \neg x_e) \\
& \wedge (\neg x_h \vee x_d \vee x_e) \wedge (x_g \vee \neg x_b) \\
& \wedge (x_g \vee \neg x_c) \wedge (\neg x_g \vee x_b \vee x_c) \\
& \wedge (\neg x_f \vee x_a) \wedge (\neg x_f \vee x_b) \\
& \wedge (x_f \vee \neg x_a \vee \neg x_b) \wedge (\neg x_d) \wedge x_a
\end{aligned}
$$

We got a CNF formula that is satisfiable if and only if the original circuit is satisfiable.

- For each gate (vertex) v in the circuit, create a variable x_v
- Case $\neg$: v is labeled $\neg$ and has one incoming edge from u (so $x_v = \neg x_u$). In SAT formula generate, add clauses $(x_u \vee x_v)$, $(\neg x_u \vee \neg x_v)$. Observe that

$$x_v = \neg x_u \text{ is true} \iff \begin{matrix} (x_u \vee x_v) \\ (\neg x_u \vee \neg x_v) \end{matrix} \text{ both true.}$$

Reduction: $CSAT \leq_P SAT$

- Case $\vee$: So $x_v = x_u \vee x_w$. In **SAT** formula generated, add clauses $(x_v \vee \neg x_u)$, $(x_v \vee \neg x_w)$, and $(\neg x_v \vee x_u \vee x_w)$. Again, observe that

$$\Big(x_v = x_u \vee x_w\Big) \text{ is true} \iff \begin{matrix} (x_v \vee \neg x_u), \\ (x_v \vee \neg x_w), \\ (\neg x_v \vee x_u \vee x_w) \end{matrix} \quad \text{all true.}$$

- Case $\wedge$: So $x_v = x_u \wedge x_w$. In **SAT** formula generated, add clauses $(\neg x_v \vee x_u)$, $(\neg x_v \vee x_w)$, and $(x_v \vee \neg x_u \vee \neg x_w)$. Again observe that

$$x_v = x_u \wedge x_w \text{ is true} \iff \begin{array}{l} (\neg x_v \vee x_u), \\ (\neg x_v \vee x_w), \\ (x_v \vee \neg x_u \vee \neg x_w) \end{array} \text{ all true.}$$

Reduction: $CSAT \leq_P SAT$

- If v is an input gate with a fixed value then we do the following. If $x_v = 1$ add clause x_v. If $x_v = 0$ add clause $\neg x_v$
- Add the clause x_v where v is the variable for the output gate

Correctness of Reduction

Need to show circuit C is satisfiable iff φ_C is satisfiable

$\Rightarrow$ Consider a satisfying assignment a for C

- Find values of all gates in C under a
- Give value of gate v to variable x_v; call this assignment a'
- a' satisfies φ_C (exercise)

$\Leftarrow$ Consider a satisfying assignment a for φ_C

- Let a' be the restriction of a to only the input variables
- Value of gate v under a' is the same as value of x_v in a
- Thus, a' satisfies C